DUAL-PORT BUFFER-TO-MEMORY INTERFACE

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for a memory system using a new memory module architecture are disclosed. In one embodiment, the memory module has two ranks of memory devices, each rank connected to a corresponding one of two 64-bit-wide data registers. The data registers connect to two 64-bit-wide ports of a 128:64 multiplexer/demultiplexer, and a 64-bit-wide data buffer connects to the opposite port of the multiplexer/demultiplexer. A controller synchronizes the operation of the data registers, the multiplexer/demultiplexer, and the data buffer.

In an operating environment, the data buffer connects to a memory bus. When a data access is performed, both ranks exchange data signaling with their corresponding data registers during a single data access. At the buffer, the memory bus data transfer occurs in two consecutive clock cycles, one cycle for each rank. This allows the memory bus transfer rate to double for the same memory bus width and memory device speed.